REMARKS

The Office Action dated August 4, 2005 has been received and carefully noted. The following remarks are submitted as a full and complete response thereto. Claims 1-16 are currently pending in the application and are respectfully submitted for consideration.

In the Office Action, claims 1-5, 8 and 16 were rejected under 35 U.S.C. §102(e) as being anticipated by Yeivin (U.S. Patent No. 6,473,808). The rejection is respectfully traversed for the reasons which follow.

Claim 1, upon which claims 2-7 are dependent, recites an interleaving method for performing parallel access in a linear and interleaved order to a predetermined number of stored data samples. The method includes the steps of storing data samples in a memory array comprising a plurality of memory devices, using a first portion of an address of the memory array to address the memory devices, using a second portion of the address to select at least one memory device to be accessed, and changing a position of the first portion and the second portion within the address, when an access order is changed between a linear order and an interleaved order.

Claim 8, upon which claims 9-15 are dependent, recites an interleaving apparatus for providing parallel access in a linear and interleaved order to a predetermined number of stored data samples. The interleaving apparatus includes a memory array with a plurality of memory devices for storing data samples. The interleaving apparatus further includes addressing means for addressing the memory devices by applying a first portion

of an address to the memory devices and by using a second portion of the address to select at least one memory device to be accessed, and change means for changing a position of the first portion and the second portion within the address in response to a change between a linear order and interleaved order.

Claim 16 recites an interleaving apparatus for providing parallel access in a linear and interleaved order to a predetermined number of stored data samples. The interleaving apparatus includes a memory array with a plurality of memory devices for storing data samples. The apparatus further includes an addresser configured to address the memory devices by applying a first portion of an address to the memory device and by using a second portion of the address to select at least one memory device to be accessed, and a changer configured to change a position of said first portion and the second portion within the address in response to a change between a linear order and an interleaved order.

Therefore, according to certain embodiments of the present invention, an interleaving method and apparatus with a parallel access to the data in linear and interleaved order are provided and can be implemented at reduced cost and chip area. According to one aspect of the present invention, by splitting the data memory into several smaller memories and changing the address portions in the interleaved order and linear order, each of the smaller memories can be accessed in linear and interleaved order without requiring multiport memory devices with several reading ports. During the linear access order, data symbols or samples of each data block can be accessed in a sequential

order from each of the memory devices one after the other, while in the interleaved access order, data samples can be randomly accessed from the memory devices. The parallel access to the plurality of memory devices can be performed in a multiplex manner using the second address portion as a multiplexing index. Then, all memory devices can be accessed in a multiplexed manner within one clock cycle, such that the number of clock cycles for parallel reading can be reduced according to the degree of multiplexing, i.e. the number of multiplexed accesses within one clock cycle.

As will be discussed below, Yeivin fails to disclose or suggest all of the elements of the claims, and therefore fails to provide the advantages/features discussed above.

Yeivin discloses a high performance communication controller for receiving, transmitting and processing high speed data streams. The communication controller includes a processor for controlling data stream transactions or frame transactions, and a memory bank, coupled to the processor, for storing data to be processed. The memory bank is disclosed as having a plurality of sections. Each section is coupled to the processor and includes a memory array for information storage, a memory selector for selecting a selected device out of the first processor, a data multiplexer for enabling the transmission of data between the selected device and the memory array, and an address multiplexer for enabling the selected device to send an address word to the memory array.

Applicants respectfully submit that Yeivin fails to disclose critical and non-obvious elements of the present claims. First, the present claims recite methods and

apparatuses for performing **parallel** access in a linear and interleaved order. Yeivin, on the other hand, merely discloses an interleaving method for performing **sequential** access to stored data. According to Yeivin, the interleaving is performed by swapping the least significant bits and the most significant bits of the address word. The first portion of the address is used to select one section from the plurality of sections contained in the memory bank and the second portion of the address is used for selecting a data word within the selected section. Thus, the interleaving is performed by sending the first portion of the address to the four most significant bits of the address bus of each memory selector, and the second address portion is sent to the address multiplexer.

According to embodiments of the present invention, on the other hand, both the interleaved and linear order may be provided. The change between the linear and the interleaved order is achieved by changing the positions of the first and of the second portion within an address, as recited in claims 1, 8, and 16. As such, according to the present invention, the interleaving means may be provided for interleaving an output address of an address counter to generate the first address portion during an interleaved access order. In particular, the interleaving means may include an address translation Read Only Memory (ROM) (Specification, paragraphs 0036-0039). In Yeivin, the swapping of bits is used to achieve interleaving but does not provide for the possibility of changing the order of access.

Additionally, Applicants respectfully submit that Yeivin fails to disclose or suggest using a second portion of the address to select at least one memory device to be

accessed, as recited in claims 1, 8, and 16. In Yeivin, the second address portion is used for the interleaving only. Whereas, according to the claimed invention the second address portion is used to select at least one memory device to be accessed when parallel access is performed. The parallel access is performed in a multiplex manner using the second address portion as a multiplexing index.

Therefore, as discussed above, Yeivin fails to disclose or suggest performing parallel access in a linear and interleaved order. Yeivin only discloses a sequential access to stored data. Yeivin fails to disclose or suggest changing between a linear order and an interleaved order and fails to disclose or suggest using a second portion of the address to select at least one memory device to be accessed. Thus, Applicants respectfully assert that Yeivin fails to disclose or suggest all of the elements of claims 1, 8, and 16. For at least the reasons discussed above, Applicants respectfully request that the rejection of claims 1, 8, and 16 be withdrawn.

Claims 2-5 are dependent upon claim 1. Consequently, claims 2-5 should be allowed for at least their dependence upon claim 1, and for the specific limitations recited therein.

Claim 6 was rejected under 35 U.S.C. §103(a) as being unpatentable over Yeivin in view of Seo (U.S. Patent Pub. No. 2003/0018942). The Office Action took the position that Yeivin discloses all of the elements of the claims, with the exception of the first portion of the address comprising ten address bits and the second portion comprising two address bits. The Office Action then relies upon Seo as allegedly curing this

deficiency in Yeivin. The above rejection is respectfully traversed for the reasons which follow.

Yeivin is discussed above. Seo discloses a memory device and method. More specifically, Seo discloses a mobile terminal including a single memory for storing data decoded by a plurality of decoder units. The terminal selects one of the decoders to decode the data and the selected decoder decodes the data. An address of a common memory connected to the decoders is determined based on information in the decoded data, and the decoded data is stored in the address of the common memory.

Applicants note that claim 6 is dependent upon claim 1. As discussed above, Yeivin fails to disclose or suggest all of the elements of claim 1. Furthermore, Seo fails to cure the deficiencies in Yeivin as Seo also fails to disclose or suggest changing between a linear order and an interleaved order and using a second portion of the address to select at least one memory device to be accessed. Therefore, the combination of Yeivin and Seo fails to disclose or suggest the elements of claim 6. In addition, claim 6 should be allowed for at least its dependence upon claim 1, and for the specific limitations recited therein.

Claim 10 was rejected under 35 U.S.C. §103(a) as being unpatentable over Yeivin in view of Schmidt (U.S. Patent Pub. No. 2002/0128037). The Office Action took the position that Yeivin discloses all of the elements of the claims, with the exception of the apparatus being one integrated system on a single chip device. The Office Action cites

Schmidt as allegedly curing this deficiency in Yeivin. The above rejection is respectfully traversed for the reasons which follow.

Yeivin is discussed above. Schmidt discloses a multi-mode wireless device on a single substrate including an analog portion and a digital portion. The analog portion includes a cellular radio core and a short-range wireless transceiver core. The digital portion includes a reconfigurable processor core coupled to the cellular radio core and the short-range wireless transceiver core.

Claim 10 is dependent upon claim 8. As discussed above, Yeivin fails to disclose or suggest all of the elements of claim 8. Furthermore, Schmidt fails to cure the deficiencies in Yeivin as Schmidt also fails to disclose or suggest changing between a linear order and an interleaved order and using a second portion of the address to select at least one memory device to be accessed. Therefore, the combination of Yeivin and Schmidt fails to disclose or suggest the elements of claim 10. In addition, claim 10 should be allowed for at least its dependence upon claim 8, and for the specific limitations recited therein.

Claims 7 and 11 were rejected under 35 U.S.C. §103(a) as being unpatentable over Yeivin in view of Merritt (U.S. Patent Pub. No. 2003/0063502). The Office Action took the position that Yeivin discloses all of the elements of the claims, with the exception of generating a first portion of the address by an address counting function. The Office Action then relies upon Merritt as allegedly curing the deficiency in Yeivin. The above rejection is respectfully traversed for the reasons which follow.

Yeivin is discussed above. Merritt discloses distributed write data drivers for burst access memories. A high speed burst mode of operation is provided where multiple sequential accesses occur following a single column address, and read data is output relative to the /CAS control signal. In the burst mode of operation the address is incremented internal to the device eliminating the need for external address lines to switch at high frequencies. Read/Write commands are issued once per burst access eliminating the need to toggle the Read/Write control line at high speeds. Only one control line per memory chip (/CAS) must toggle at the operating frequency in order to clock the internal address counter and the data input/output latches.

Claims 7 and 11 are dependent upon claims 1 and 8, respectively. As discussed above, Yeivin fails to disclose or suggest all of the elements of claims 1 and 8. Furthermore, Merritt fails to cure the deficiencies in Yeivin as Merritt also fails to disclose or suggest changing between a linear order and an interleaved order and using a second portion of the address to select at least one memory device to be accessed. Therefore, the combination of Yeivin and Merritt fails to disclose or suggest the elements of claims 7 and 11. In addition, claim 7 and 11 should be allowed for at least its dependence upon claim 1 and 8, respectively, and for the specific limitations recited therein.

Claim 9 was rejected under 35 U.S.C. §103(a) as being unpatentable over Yeivin in view of Suzuki (U.S. Patent Pub. No. 20030225985). The Office Action took the position that Yeivin discloses all of the limitations of the claim, with the exception of the

use of single-port RAM devices. The Office Action then relies upon Suzuki as allegedly curing the deficiency in Yeivin. The above rejection is respectfully traversed for the reasons which follow.

Yeivin is discussed above. Suzuki discloses an interleaver for iterative decoder. Each of the entire interleaver memory and the entire interleaver pattern memory is broken into two separate memory portions that are each implemented using single port memory structures. One of the memory structures is employed for odd address locations, and another memory structure is employed for even address locations.

Claim 9 is dependent upon claim 8. As discussed above, Yeivin fails to disclose or suggest all of the elements of claim 8. Furthermore, Suzuki fails to cure the deficiencies in Yeivin as Suzuki also fails to disclose or suggest changing between a linear order and an interleaved order and using a second portion of the address to select at least one memory device to be accessed. Therefore, the combination of Yeivin and Suzuki fails to disclose or suggest the elements of claim 9. In addition, claim 9 should be allowed for at least its dependence upon claim 8, and for the specific limitations recited therein.

Claims 8 and 15 were rejected under 35 U.S.C. §103(a) as being unpatentable over Shiu (U.S. Patent No. 6,392,572) in view of Yeivin. The Office Action took the position that Shiu teaches a buffer architecture for a turbo decoder comprising a turbo interleaver but fails to disclose an apparatus as described in the present claims. The Office Action

then relies upon Yeivin as allegedly curing this deficiency in Shiu. The above rejection is respectfully traversed for the reasons which follow.

Yeivin is discussed above. Shiu discloses a buffer architecture for a turbo decoder. The buffer is partitioned into a number of banks, with each bank being independently accessible. In order to avoid access contentions, the banks are assigned to the rows and columns of a 2-dimensional array used for code interleaving such that APP data for consecutive bits are accessed from different banks. In order to support "linear" addressing, the banks can be arranged into two sets, which are assigned to even-numbered and odd-number columns of the array. For supporting "interleaved" addressing, the banks can be assigned to groups of rows of the array such that adjacent rows in the interleaved array are assigned to different groups.

Applicants respectfully submit that Shiu and Yeivin, whether viewed singly or combined, fails to disclose or suggest performing parallel access in a linear and interleaved order, changing between a linear order and an interleaved order, and using a second portion of the address to select at least one memory device to be accessed, as recited in claim 8. Thus, the combination of Shiu and Yeivin fails to render claim 8 obvious.

Claim 15 is dependent upon claim 8. As such, claim 15 should be allowed for at least its dependence upon claim 8, and for the specific limitations recited therein.

The Office Action indicated that claims 12-14 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form

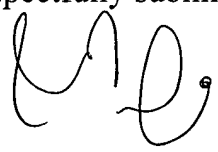
including all of the limitations of the base claim and any intervening claims. As discussed above, Applicants respectfully submit that the claims are allowable in their current form. Therefore, claims 12-14 have not been amended to be in independent form.

Applicants respectfully submit that the cited prior art fails to disclose or suggest critical and important elements of the claimed invention. These distinctions are more than sufficient to render the claimed invention unanticipated and unobvious. It is therefore respectfully requested that all of claims 1-16 be allowed, and this application passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicants respectfully petition for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,



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